UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/872,209	06/01/2001	R. Daniel McGrath	ATM-181	1987

3897 7590 12/30/2003

SCHNECK & SCHNECK
P.O. BOX 2-E
SAN JOSE, CA 95109-0005

EXAMINER	
YAM, STEPHEN K	
ART UNIT	**PAPER NUMBER**
2878	

DATE MAILED: 12/30/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

UNITED STATES PATENT AND TRADEMARK OFFICE

COMMISSIONER FOR PATENTS
UNITED STATES PATENT AND TRADEMARK OFFICE
P.O. BOX 1450
ALEXANDRIA, VA 22313-1450
www.uspto.gov

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Paper No. 14

Application Number: 09/872,209
Filing Date: June 01, 2001
Appellant(s): MCGRATH ET AL.

Kwan Chan
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed October 10, 2003.

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

Appellant's brief includes a statement that claims 1-9 do not stand or fall together and provides reasons as set forth in 37 CFR 1.192(c)(7) and (c)(8).

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

EP 0942592	Shinohara	10-1999
5,760,636	Noble et al.	6-1998

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shinohara European Patent Application No. EP-0942592 in view of Noble et al. US Patent No. 5,760,636.

Shinohara teach (see Fig. 4) an integrated imager system having an array of pixel areas (30) with at least one control area (4), wherein said pixel areas include a plurality of light collecting elements (see Col. 3, lines 1-6) which each receive and store electronic information in an amount indicative of an amount of light received during an integration period, with the control area having an internal timing element (7), with an interface (3, 6, 10, 13, 20) for receiving a plurality of data, address, and control signals, said interface receiving a mode signal (10) (see Col. 3, lines 19-23) for setting the system in one of a first operating mode or a second operating mode characterized in that the first operating mode uses (see Col. 4, lines 3-9) the internal timing element (7) to control timing operation of the system and the second operating mode bypasses (see Col. 4, lines 20-22) the internal timing element to control timing operation of the system. Regarding Claim 2, Shinohara teach (see Fig. 4) the control area including a data bus (20), an address and control bus (3) (see Col. 3, lines 54-58) electrically coupled to the interface and a bypass multiplexer (9) connected to the control bus, said multiplexer operating to interconnect the internal timing element (7) to the control bus upon receipt of a first mode signal and operating to bypass the internal control element upon receipt of a second mode signal (see Col. 3, lines 19-23). Regarding Claim 3, Shinohara teach (see Fig. 4 and Col. 4, lines 20-22) means for receiving timing signals from an external timing element (2) when the system is operating in the second operating mode. Regarding Claim 4, Shinohara teach (see Fig. 4 and Col. 4, lines 29-33) the external timing block (2) including a color recovery block. Since Shinohara teach (see Col.

3, lines 8-10) the external timing element (2) outputting drive pulses for the second operating mode, it is inherent that the external timing element (2) includes an external timing generator. Regarding Claim 5, Shinohara teach (see Fig. 4) the external timing block (2) comprising a microcomputer. It is inherent that a microcomputer includes a memory for data storage and a DMA interface block for controlling external devices. Regarding Claim 6, Shinohara teach (see Col. 3, lines 24-29) the imager operating in the first operating mode when the interface is not connected to receive the mode signal. Shinohara does not teach the interface as a user interface configured to receive the mode signal from a user. Noble et al. teach (see Fig. 1) a microprocessor (10) with a user interface (12) wherein the clock frequency ("Clock Frequency") is adjusted based on a mode signal (SLOW#) received from a user (see Col. 3, lines 46-49 and Col. 6, lines 21-29) to provide user control of power consumption (see Col. 6, lines 24-29). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a user interface receiving a mode signal from a user as taught by Noble et al. in the system of Shinohara, to provide customized user control of power consumption to best suit a user's particular needs, as taught by Noble et al. (see Col. 6, lines 26-29).

Claims 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shinohara.

Shinohara teach (see Fig. 3) a timing selector for an integrated imager, comprising an onboard timing means (7) associated with a integrated imager (1), for providing standard timing signals to operate a clock circuit (7, 8, 21) aboard the integrated imager (1) and an outboard logic circuit (2) electrically connected to the integrated imager generating signals for establishing timing signals for customized imager operation. Shinohara also teach the outboard logic circuit (2) performing (see Col. 4, lines 29-33) image signal processing such as color processing, white

balancing, etc., and turning off the microcomputer to save power (see Col. 4, lines 34-40). Regarding Claim 8, Shinohara teach (see Fig. 3) the outboard logic unit (2) outputting drive pulses- therefore, it is inherent that the outboard logic unit (2) includes means for generating clock signals for bypassing the clock circuit (see Col. 3, lines 44-51). Regarding Claim 9, Shinohara teach (see Fig. 3 and Col. 3, lines 24-29) the outboard logic circuit having means (10) for generating clock signals using the clock circuit (7, 8, 21). Shinohara do not teach a user establishing timing signals and a user interface allowing selection of the onboard timing means or outboard logic circuit. It would have been obvious to one of ordinary skill in the art at the time the invention was made to establish a user interface to allow selection of the onboard timing means or outboard logic circuit and allow a user to establish timing signals in the timing selector of Shinohara, to allow user control of power consumption from the microprocessor and activation/deactivation of the image processing functions provided by the microprocessor to provide a more user-flexible system.

(11) Response to Argument

Applicant argues that the claimed invention has 2 full operating modes wherein one mode utilizes an internal timing element while the other mode utilizes an externally provided timing element. Examiner asserts that while Shinohara discusses a first mode of operation as a "preliminary operation" (see Col. 4, lines 34-45), it is still an operating mode which "utilizes an internal timing element to control timing operation of the system", as recited in Claim 1, as described by Shinohara, by using a reference clock generation circuit 7 located internally with the imager system 1. Since the imager operates in the preliminary mode to provide low-

resolution readout and intermittent operations (see Col. 4, lines 40-43), it is fully functional to provide imaging data and provide working operation of the system.

Applicant also argues that Noble does not teach bypassing the internal timing element to externally control the timing operation of the system, but instead increases and decreases the clock frequency and thus, a voltage to a microprocessor, and hence, cannot be used for the system of Shinohara. Examiner asserts that Shinohara already teaches the bypassing of the internal timing element (using switch 9) to externally control the timing operation of the system, (see Col. 4, lines 20-22), and that Noble is used as a secondary reference to provide teachings of the user control of a system clock frequency compared to an automatic control of the clock frequency in Shinohara. The particular workings of Noble are not utilized for the combination, but rather the suggestions for allowing a user interface to control the clock frequency operation of the system, thereby enhancing power conservation while sacrificing the operating performance of the system (through lower clock frequency). Therefore, by combining such teachings of Noble to establish *user-control* for the switch 9 in Shinohara, a user determines the optimal trade-off between power consumption and performance, and therefore is able to establish increased control over the system according to a desired operation.

Applicant further argues with respect to Claims 7-9 that it would not have been obvious to provide a user interface for controlling the timing of the system of Shinohara, as the current system provides automated switching between the reference timing signal (standard timing signal) on the onboard timing means 7 and the user defined timing signal from an outboard logic circuit 2. Examiner asserts that providing user control of an operation of imaging displays, especially to affect power consumption in a portable environment, is well known in the art, such

as in the displays of laptops, digital cameras, and PDA devices, wherein a user can control the operating brightness of the screen to reduce energy consumption, thereby sacrificing the performance of the screen through decreased visibility. Such a motivation can be applied to any electronic device, such as Shinohara, which already teaches two operating modes, one of which conserves power through diminished performance (low-resolution readout and intermittent operation) (see Col. 4, lines 34-45), and the other providing full performance. Such a modification permits enhanced user operation by increasing the versatility of the system.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

SY

SY
December 22, 2003

THANH X. LUU
PATENT EXAMINER

Conferees
Stephen Yam
Olik Chaudhuri
David Porta

LAW OFFICE OF THOMAS SCHNECK
P.O. BOX 2-E
SAN JOSE, CA 95109-0005